Project ID # elt246

Implementation of WBG devices in circuits, circuit topology, system integration as well as SiC devices

Principal Investigator: Prof. Anant Agarwal (PI)

Prof. Jin Wang (Co-PI)

The Ohio State University

Department of Electrical and Computer Engineering

Center for High Performance Power Electronics

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2020 DOE Annual Merit Review

Overview

Timeline

- Project start April 2019
- Project end March 2024
- Percent Complete: 20%

Barriers

- Commercial devices are not ready for insertion into a vehicle power train for long operational life.
- A comprehensive reliability study will be undertaken to address various weaknesses in currently available commercial devices.

Budget

- Total project funding: $ 1.5 M

  BP1 funding: $ 300 K

  BP2 funding: $ 300 K

Partners

- Sandia National Laboratories
- SUNY POLYTECHNIC INSTITUTE

Relevance - background

Background

- SiC devices are NOT reliable and rugged as required in automotive applications for operational life of 300,000 hrs and create new device designs to address various weaknesses in currently available commercial devices.
- In order to reduce cost, all device vendors have sacrificed reliability/ruggedness to cut cost.
- Short channel length reduces device size and cost but at the expense of reduced short-circuit time of 2-3 μs.
- The gate oxide thickness has been thinned to 30 - 40 nm without reducing the gate voltage in order to reduce device size/cost.
- **Commercial devices, available to-date, are not suitable for insertion into a vehicle power train for long operational life.**
- A comprehensive reliability study will be undertaken for commercially available devices both as discrete devices and in an inverter to uncover failures such as threshold voltage instability, inadequate short circuit time, gate oxide failures, as well as body diode instability.

Relevance - objectives / impact

Overall objectives in this project:

- Reliability/ruggedness evaluation of SiC MOSFETs in stand alone as discrete and in a 10 kW inverter.
- The new designs will be implemented/improved every year through extensive testing by OSU in collaboration with SUNY POLY

Objectives in previous period (BP1, FY2019-2020):

- **Reliability/ruggedness evaluation** of Discrete commercial SiC devices
- **A three phase Inverter (Inverter-1) will be designed & built** with reduced ratings (10 kW) using discrete commercial MOSFETs to test the devices under realistic drive cycles

Objectives in this period (BP2, FY2019-2020):

- **Ruggedness of Gen-1 MOSFETs from SUNY Polytechnic** will be evaluated
- **An improved three phase Inverter (Inverter-2) will be built using Gen-1 MOSFETs** to test the devices under realistic drive cycles

Impact of research:

- The successful development of the project will result in a highly efficient and reliable power devices and power electronics suitable for the automotive applications.

Milestones – BP1

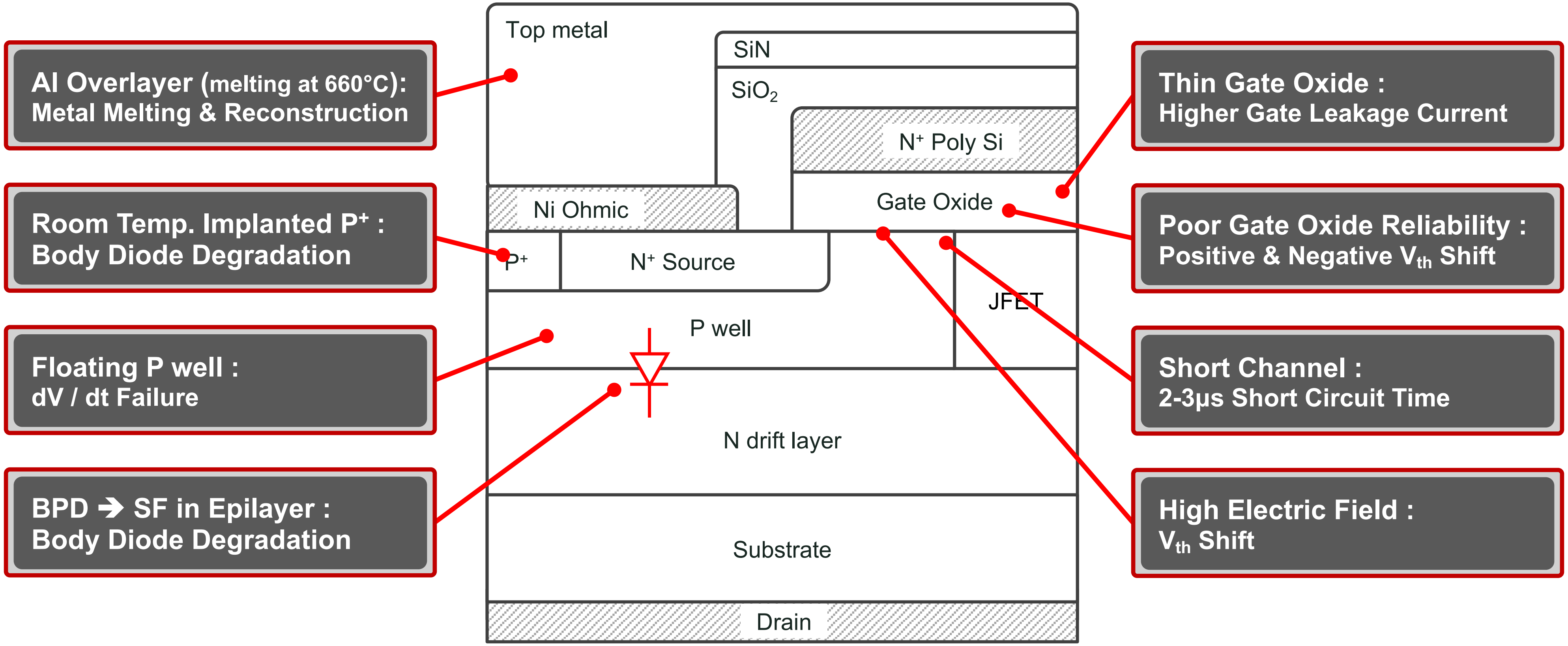
Milestone	Type	Description
Commercial devices secured, and test platform prepared.	Technical	Test platform established for failure mechanism tests. **Completed**
Device failure mechanism tests completed.	Technical	Gate oxide leakage current, body diode stability, threshold voltage stability, short circuit time and avalanche energy tests of commercial SiC MOSFETs. **Completed**
Failure points in commercial devices identified and mitigation planned.	Technical	Weaknesses in commercial devices are uncovered through accelerated testing and 2D simulations are performed to strengthen the failure points by design of devices. **Completed**
10 kW Inverter-1 design and build completed with the inputs from the device evaluation results.	**Go/No Go**	Inverter-1 is fully designed and built to evaluate the state-of-the-art commercial SiC devices under three phase operation conditions. **Completed**

Milestones – BP2

Milestone	Type	Description
Gen-1 devices are received and packaged for reliability testing	Technical	Gen-1 devices from SUNY POLY are packaged and preliminary electrical tests performed to get ready for accelerated stress.
Stand-alone device failure mechanism tests on Gen-1 devices completed	Technical	Gate oxide leakage current vs. gate voltage, body diode stability, threshold voltage stability, short circuit time and avalanche energy tests of Gen-1 SiC MOSFETs from SUNY POLY
Gen-1 devices evaluated with Inverter-1	Technical	Gen-1 devices from SUNY POLY fully evaluated with the Inverter-1 at accelerated temperature and power cycles
Inverter-2 built and debugged	**Go/No Go**	Inverter-2 fully built and debugged with Gen-1 SiC devices from SUNY POLY with 15% higher power density

Approach

Reliability/ruggedness evaluation of discrete SiC MOSFETs



I. **Yu *et al.*, Bias-induced Threshold Voltage Instability and Interface Trap Density Extraction of 4H-SiC MOSFETs**, Proc. on 7th IEEE Workshop on Wide Bandgap Power Devices and Applications, 2019

II. **Kang *et al.*, Body Diode Reliability of Commercial SiC Power MOSFETs**, Proc. on 7th IEEE Workshop on Wide Bandgap Power Devices and Applications, 2019

III. **Liu *et al.*, Gate Leakage Current and Time-Dependent Dielectric Breakdown Measurements of Commercial 1.2 kV 4H-SiC Power MOSFETs**, Proc. on 7th IEEE Workshop on Wide Bandgap Power Devices and Applications, 2019

Approach

Gen 1~4 devices fully evaluated with the Inverter

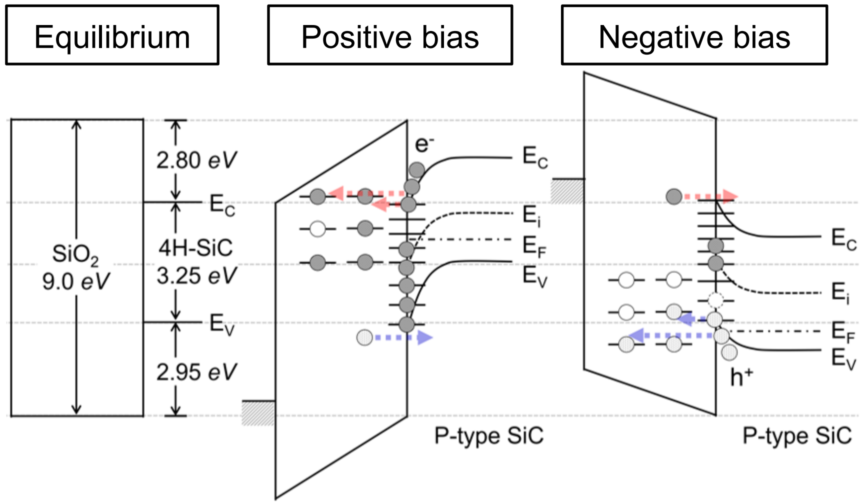
- Failure mechanism evaluation results: Commercial devices, Gen-1 ~ Gen-4 from SUNY
- Test results from the inverter-based device evaluations

Budget Period	Ruggedness test of SiC devices in stand-alone mode and in Inverter by OSU	Inverter Build by OSU	Device Design and Fabrication by SUNY Poly
BP1	Test Commercial devices: Stand-alone	Build **Inverter-1** using Commercial devices	**Gen-1**
BP2	Test **Gen-1** devices: Stand-alone and using **Inverter-1**	Build **Inverter-2** using **Gen-1** devices	**Gen-2**
BP3	Test **Gen-2** devices: Stand-alone and using **Inverter-2**	Build **Inverter-3** using **Gen-2** devices	**Gen-3**
BP4	Test **Gen-3** devices: Stand-alone and using **Inverter-3**	Build **Inverter-4** using **Gen-3** devices	**Gen-4**
BP5	Test **Gen-4** devices: Stand-alone and using **Inverter-4**	Build **Inverter-5** using **Gen-4** devices	**Gen-5** (Suitable for automotive market)

Technical Accomplishments and Progress

Reliability evaluation of SiC devices – Large variability among vendors

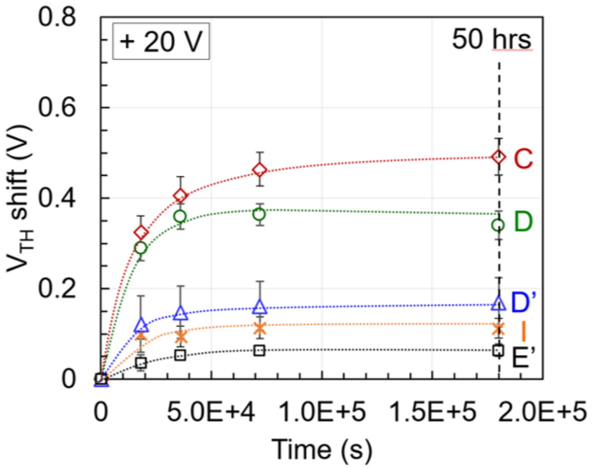
A. Threshold Voltage Stability: V_G = +20 V, +30V, -10 V

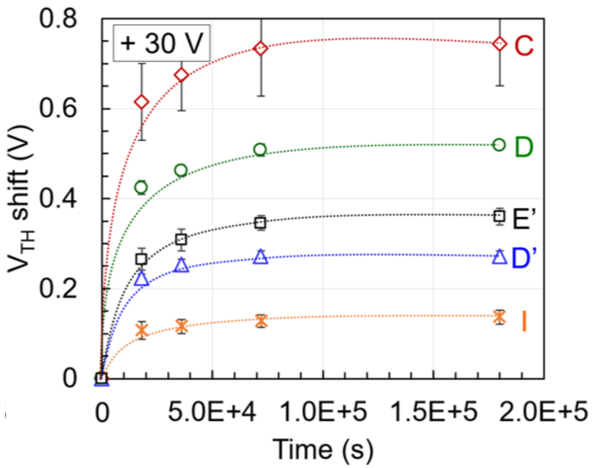


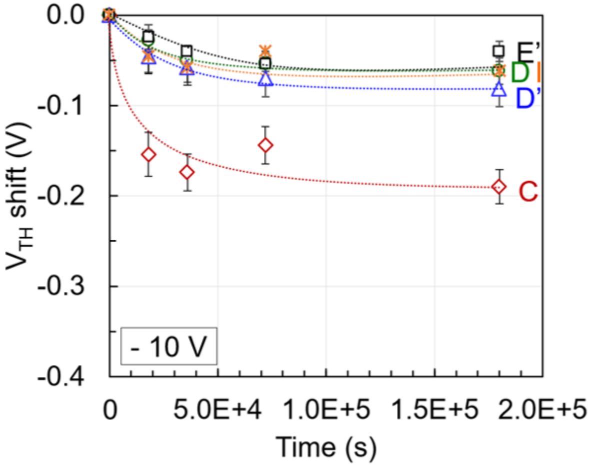
Bias-stress on the gate gives rise to injection of carriers into the gate oxide by direct tunneling to the near interface traps.

This is indicative of defects in oxide.

Concern for automotive companies for long-term reliability.





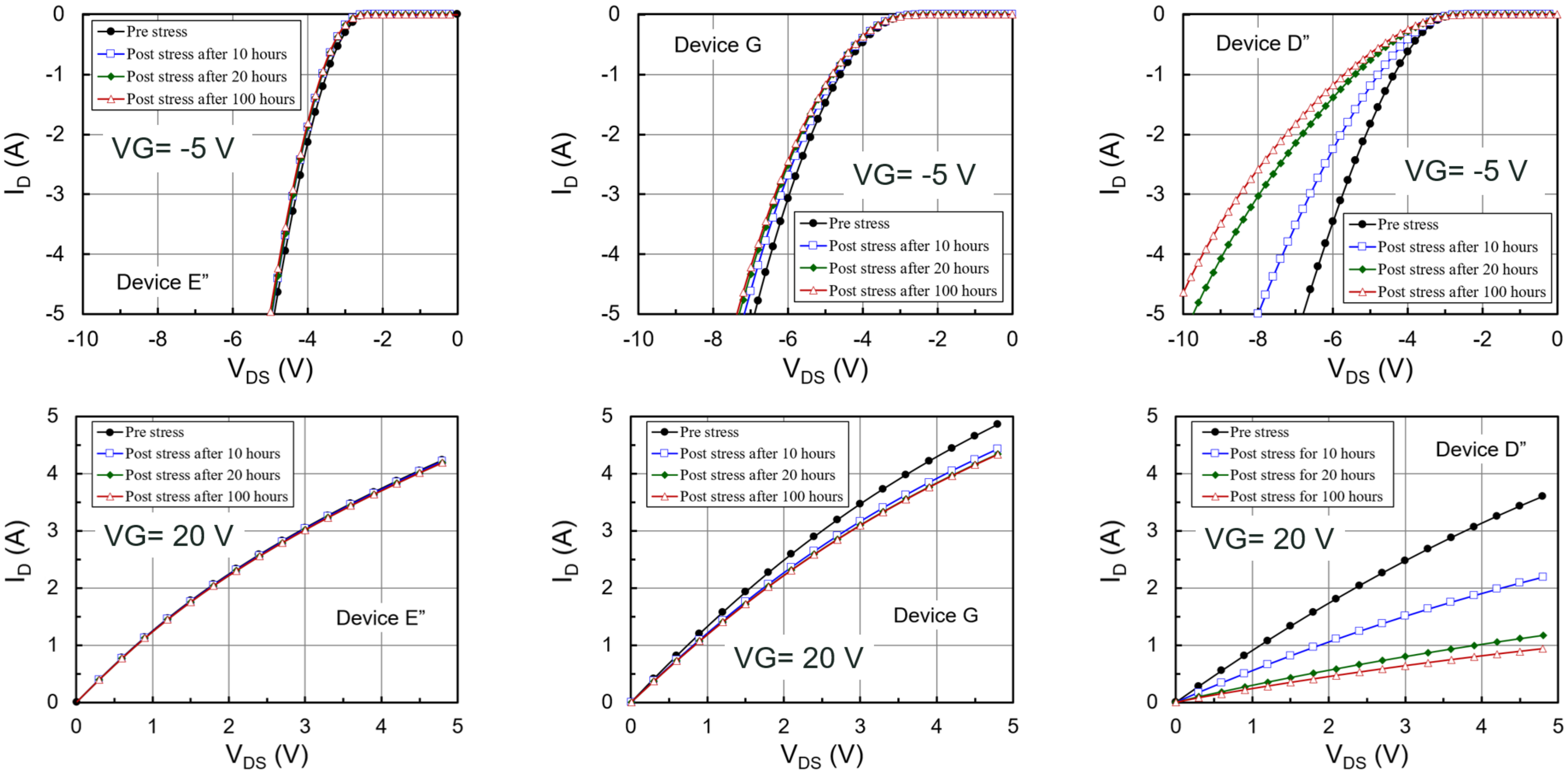


Technical Accomplishments and Progress

Reliability evaluation of SiC devices – Large variability among vendors

B. Body Diode Degradation on 1700 V devices

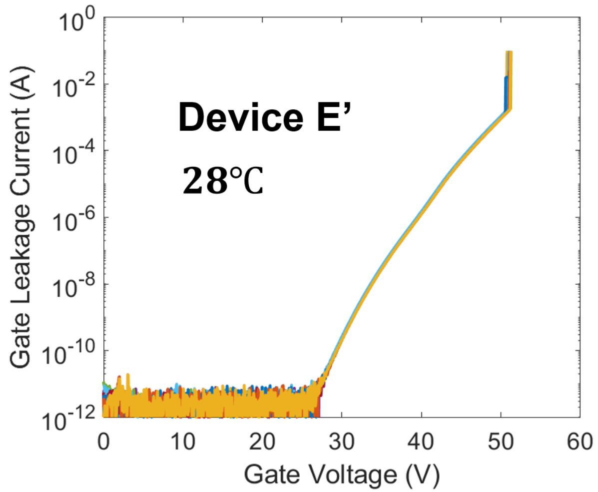
- All tested devices (Device D") are degraded after forward body diode stress. **Big concern for reliability.**

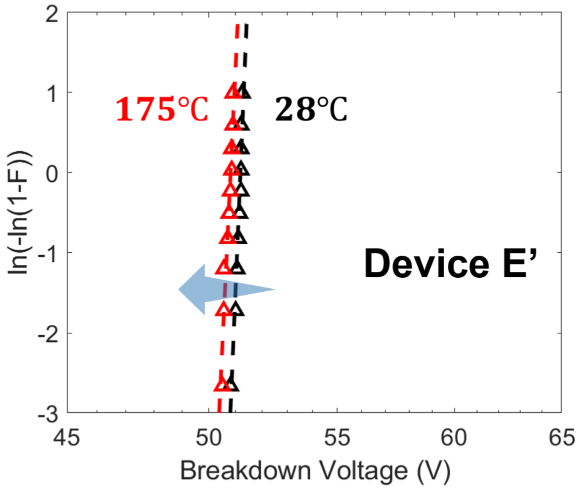


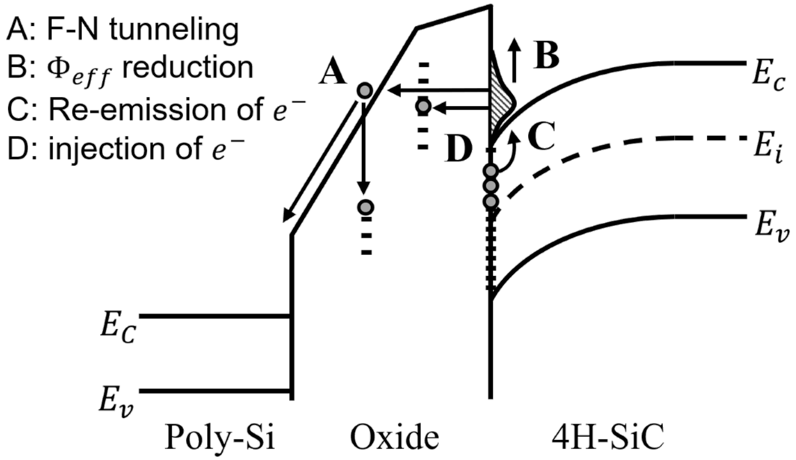
Technical Accomplishments and Progress

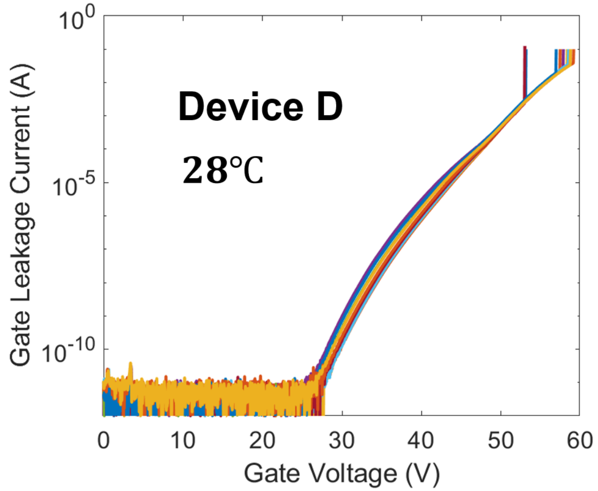
Reliability evaluation of SiC devices – Large variability among vendors

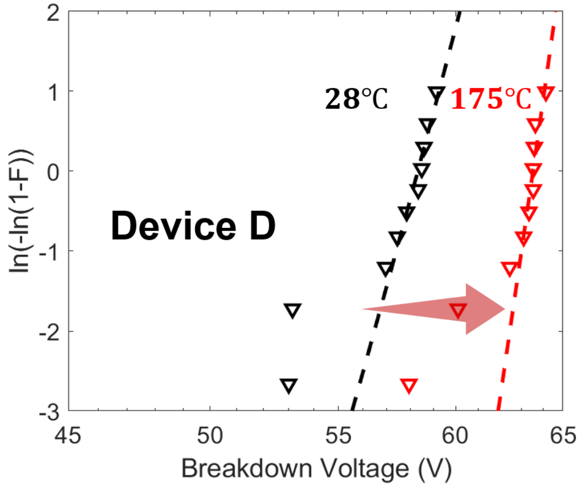
C. Gate Oxide Leakage Current – Defects in gate oxide











Device E': Process C is dominant

➔ There is no significant amount of near interface oxide traps

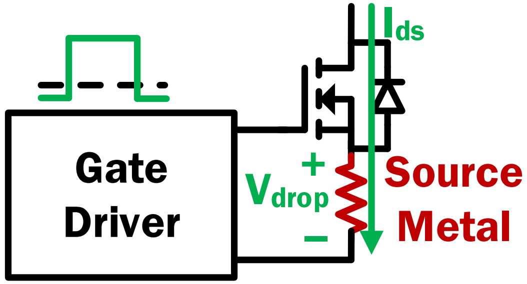
Device D: Process D is dominant

➔ There are significant amounts of near interface oxide traps

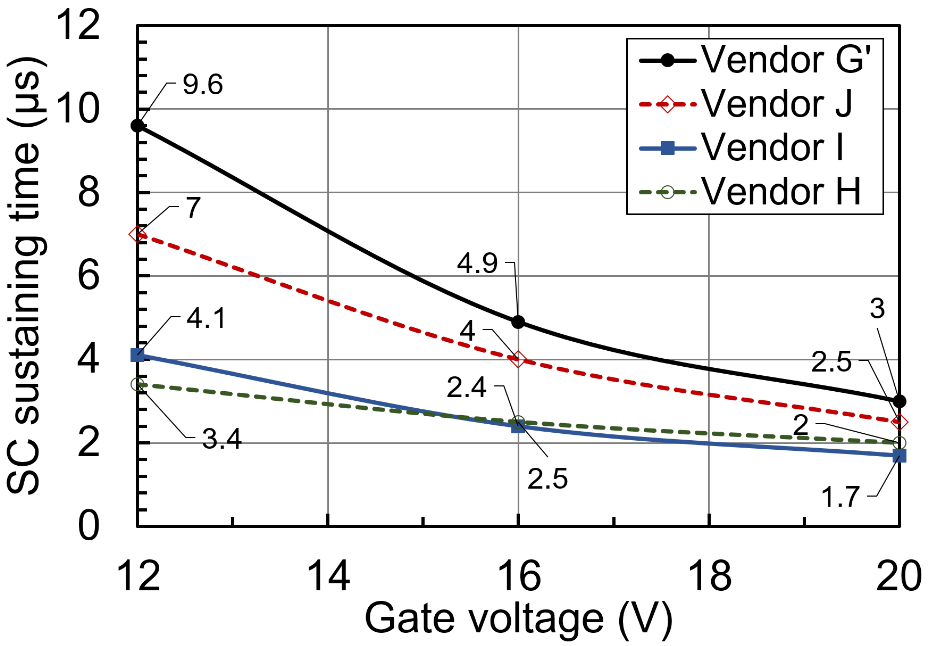
Technical Accomplishments and Progress

Reliability evaluation of SiC devices – Large variability among vendors

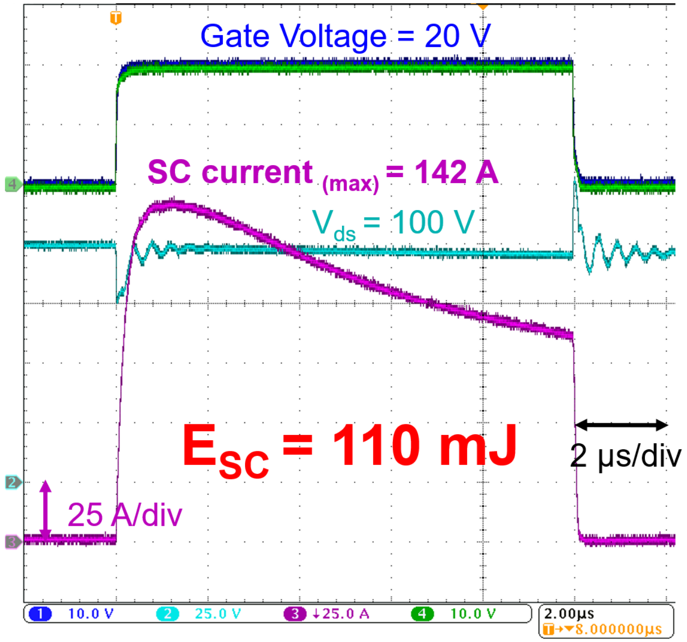
D. Short Circuit Time – Too short! Concern for reliable operation

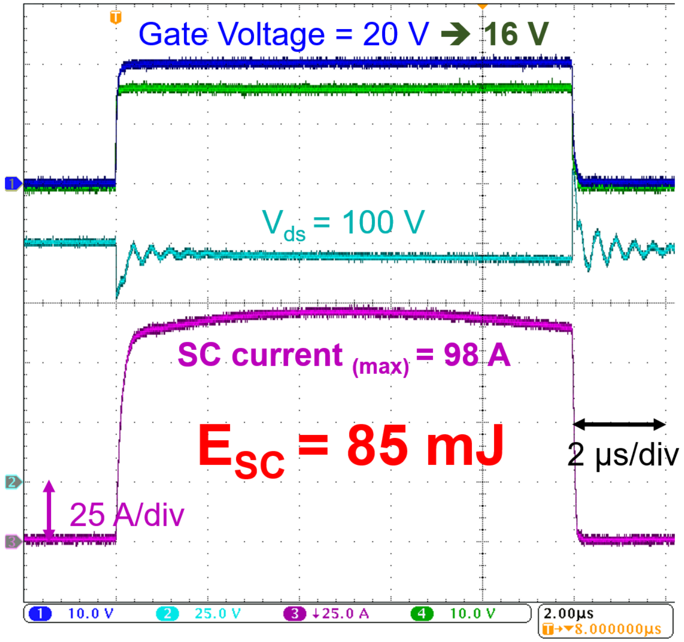


SC time vs. Gate voltage



SC Test with External Rs



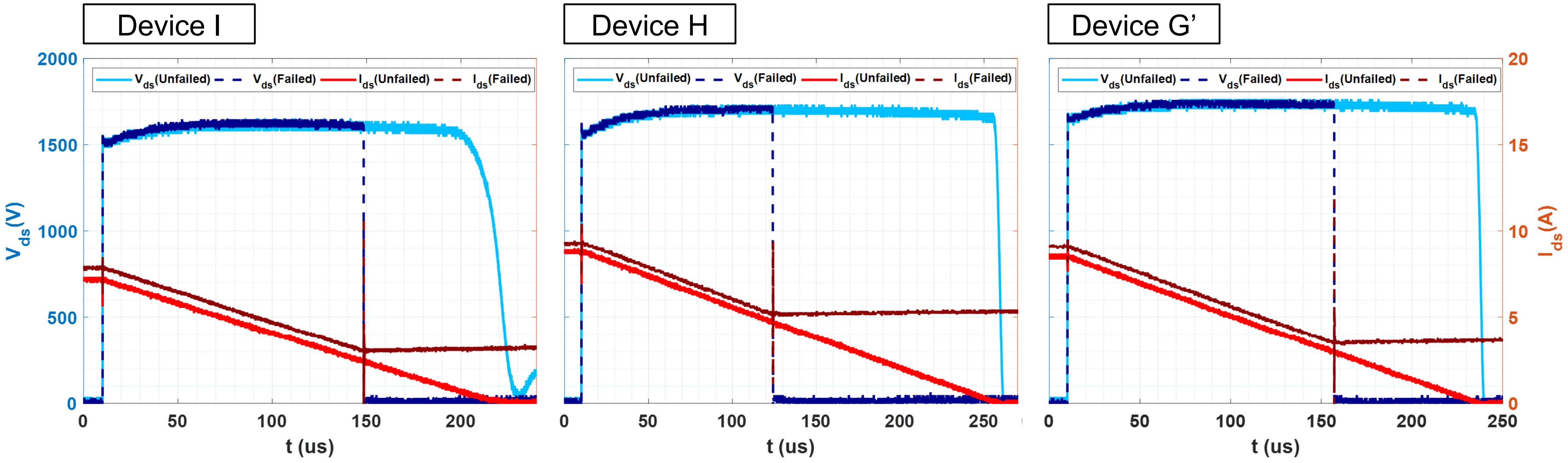


Technical Accomplishments and Progress

Reliability evaluation of SiC devices – Large variability among vendors

E. Avalanche Energy – Good

	Device I	Device H	Device G’
Failed Case	1.20 J	1.59 J	1.59 J
NOT-failed Case	1.19 J	1.82 J	1.64 J



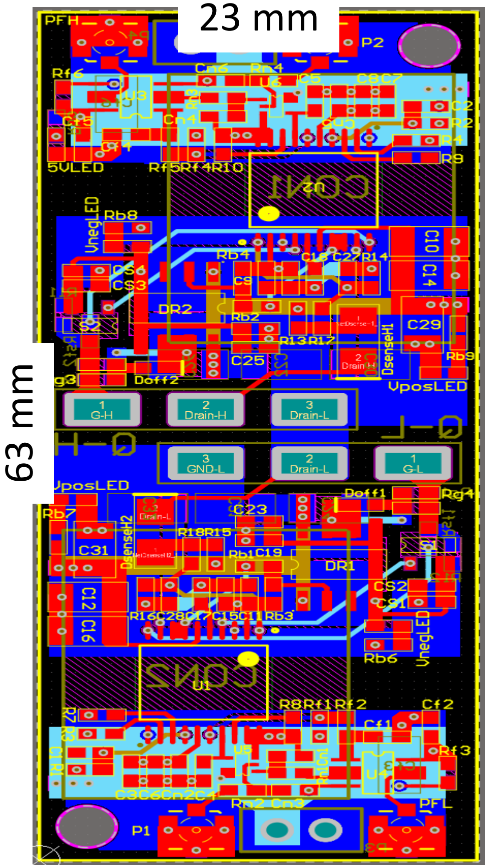
Technical Accomplishments and Progress

10 kW 3-phase Inverter development using commercial SiC MOSFETs

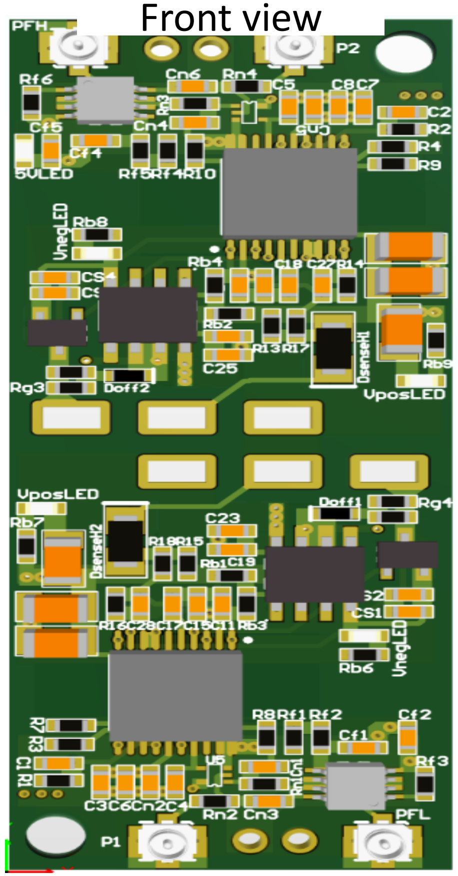
A. Gate Driver Layout Design

Prof. Jin Wang, OSU

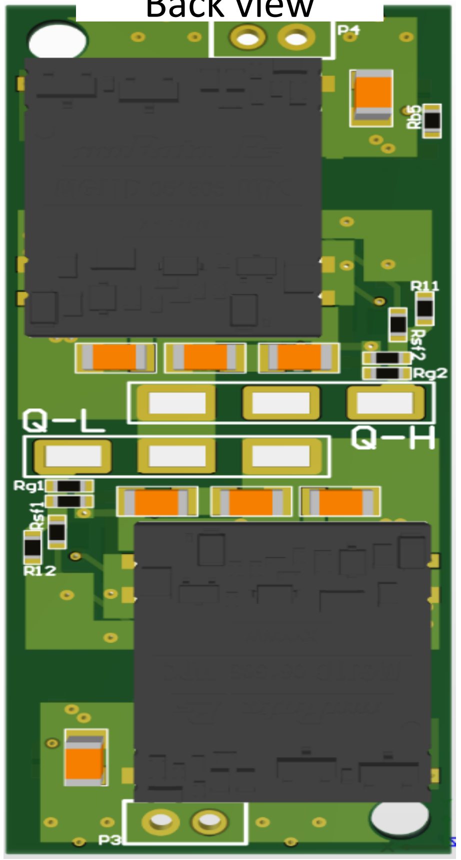
- Short circuit protection
- Coaxial connector to mitigate EMI interface



Front view



Back view



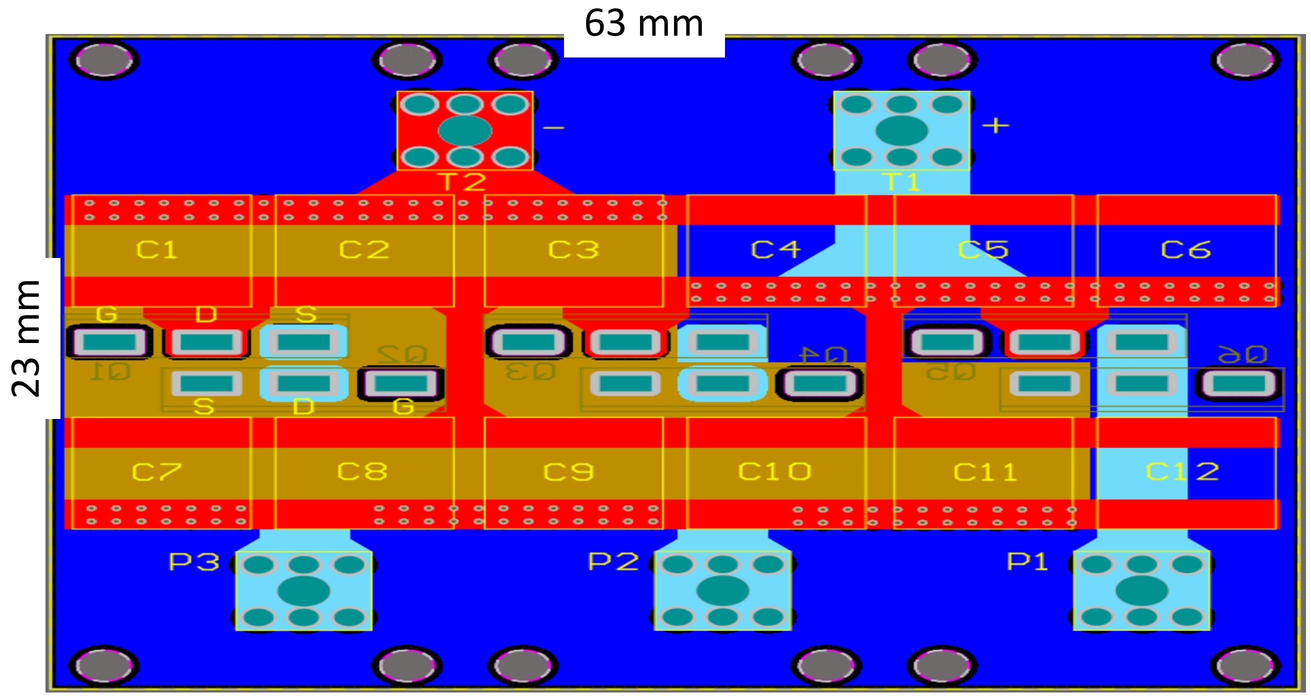
Technical Accomplishments and Progress

10 kW 3-phase Inverter development using commercial SiC MOSFETs

B. Power Board Design

Prof. Jin Wang, OSU

- Nominal Output power: 10 kW
- Nominal Input voltage: 800 V
- Target Efficiency: 99%
- Target Power Density: 100 kW/L



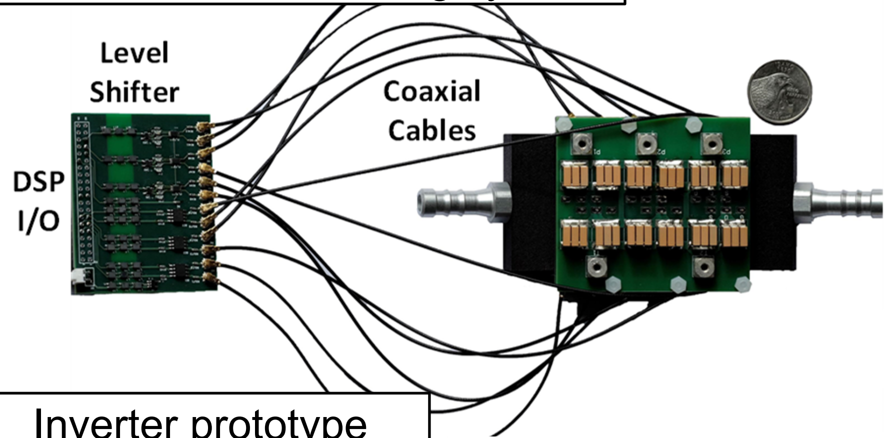
Technical Accomplishments and Progress

10 kW 3-phase Inverter development using commercial SiC MOSFETs

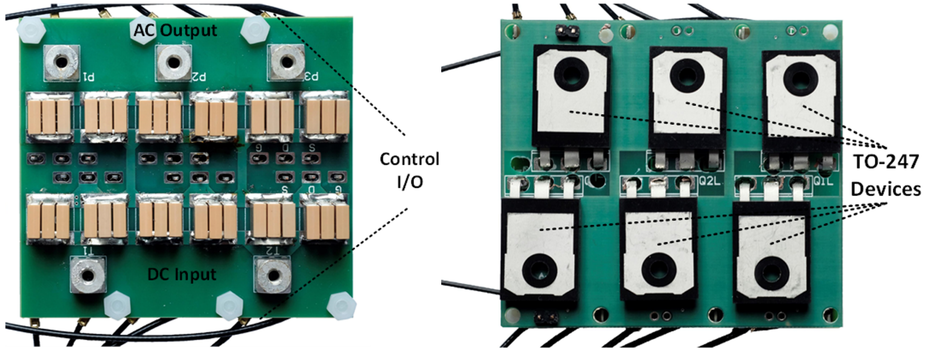
C. 10 kW Three Phase Inverter – Built and Tested

Prof. Jin Wang, OSU

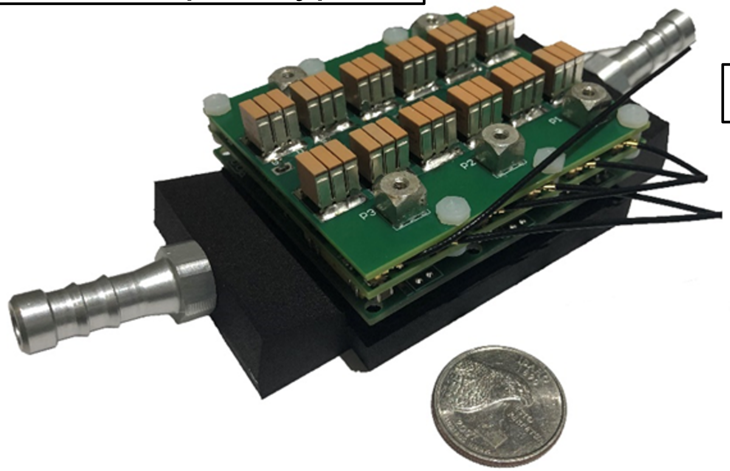
Inverter circuit & cooling system



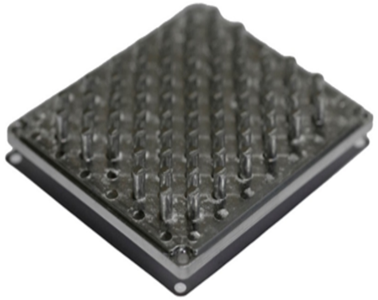
Inverter front & back view



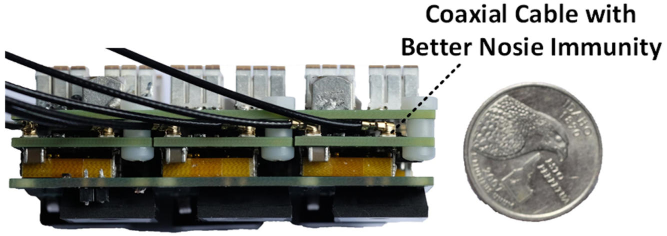
Inverter prototype



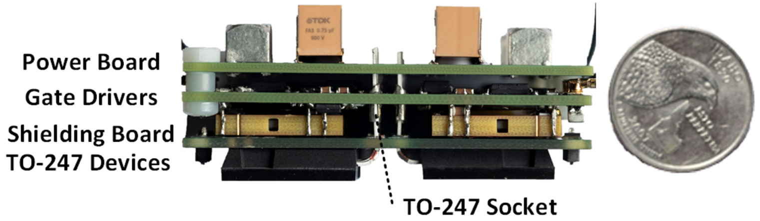
Cooling pad



Detail view



Inverter Side View (A)



Inverter Side View (B)

Collaboration and Coordination

Sandia National Laboratories

SNL will participate in the **design reviews of the SiC MOSFETs and inverters** and coordinate efforts between the SUNY Poly and OSU team and other project teams within the consortium.

SUNY

SUNY Polytechnic to strengthen the ruggedness of **SiC 1200 V, Gen 2-4 devices** to achieve failure rates much less than Si devices

THE OHIO STATE UNIVERSITY

Reliability/ruggedness evaluation of SiC devices from SUNY Polytechnic by individually testing them and then **evaluate them in a 10 kW, 3 phase inverter system** built with a specific purpose of stressing devices

Remaining Challenges and Barriers

- **SiC cost needs to be less than 3 cents/A for automotive application**
- **Short Circuit Time should be at least 10 μs**
- **Body diode should be stable**
- **Threshold voltage shift should be less than 50 mV at room temperature wit h V_G = 25 V**
- **Gate oxide leakage current should increase with temperature according to physics with minimum oxide traps.**

Proposed Future Research

Gen-1 devices will be received and packaged for reliability testing:

Gen-1 devices from SUNY POLY will be packaged and preliminary electrical tests will be performed to get ready for accelerated stress

Stand-alone device failure mechanism tests on Gen-1 devices:

Gate oxide leakage current vs. gate voltage, body diode stability, threshold voltage stability, short circuit time and avalanche energy tests of Gen-1 SiC MOSFETs

Gen-1 devices will be evaluated with Inverter-1:

Gen-1 devices fully will be evaluated with the Inverter-1 at accelerated temperature and power cycles

Inverter-2 will be built and debugged with Gen-1 SiC devices

Summary

- We evaluated reliability of discrete commercial SiC devices and built 10 kW three phase inverter.
- The reliability *wrt* gate oxide, short circuit, V_{th} shift, body diode is NOT adequate.
- Commercial devices, available today, are NOT suitable for 300,000 hrs operation in automotive inverter.
- We will evaluate Gen-1 devices with 10 kW inverter.
- We will work with SUNY Poly to re-design more reliable devices